Page 2, line 10, delete ",".

IN THE CLAIMS

Please amend the claims as follows:

1. (Amended) A programmable device comprising:

means for storing programmable information; and

means for providing a plurality of output clocks each capable of oscillating at a different one of a plurality of frequencies, said output frequencies generated in response to (i) a reference clock frequency and (ii) one or more programming inputs.

2. (Amended) The circuit according to claim [1] ~~1~~2 wherein said plurality of output clocks are individually programmable to [a] oscillate at a different one of said plurality of frequencies.

3. (Amended) The circuit according to claim [2] ~~1~~2 wherein said [means for providing said plurality of output clocks] second circuit comprises a phase lock loop (PLL).

4. (Amended) The circuit according to claim [1] ~~1~~ 2 wherein said plurality of output [clock is] clocks are accessible through one or more input/output pins.

5. (Amended) The circuit according to claim [1] ~~1~~ 2 wherein said output clocks have [a particular] an impedance that may be adjusted in response to said one or more programming inputs to match the impedance of an external device.

6. (Amended) The circuit according to claim [1] ~~1~~ 2 wherein said output frequencies can be programmed after fabrication and installation of said programmable device.

7. (Amended) The circuit according to claim [1] ~~1~~ 2 wherein said reference clock frequency [comprises] is selected from one or more reference clock frequencies in response to (i) a multiplexer and (ii) a configuration signal.

8. (Amended) The circuit according to claim 7 wherein said [inputs to said multiplexer] one or more reference clock frequencies are [derived from one or more internally generated clocks] generated internally to said programmable device.

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9. (Amended) The circuit according to claim 7 wherein said [inputs to said multiplexer] one or more reference clock frequencies are [derived from one or more externally generated clocks] generated externally to said programmable device.

10. (Amended) A device selected from the group consisting of programmable logic devices (PLDs), complex programmable logic devices (CPLDs) and field programmable gate arrays (FPGAs), comprising the circuit of claim [1] 12.

11. (Amended) The circuit according to claim 1 wherein an input delay and an output delay are reduced to zero in response to said programming inputs.

12. (Amended) A programmable device comprising:

a first circuit capable of storing programmable information; and

a second circuit capable of providing a plurality of output [clock] clocks each capable of oscillating at a different one of a plurality of frequencies, said output clocks generated in response to (i) a reference clock frequency[, said second circuit comprising a phase locked loop (PLL)] and (ii) one or more programming inputs.

13. (Amended) The circuit according to claim [12] 1 wherein said plurality of output [clock] clocks are individually programmable to [a] oscillate at one of said plurality of frequencies.

14. (Amended) The circuit according to claim 13 wherein said clocks have [a particular] an impedance that may adjusted in response to said one or more programming inputs to match the impedance of an external device.

12 ~~15~~. (Amended) A method for providing an integrated programmable device and clock generation circuit comprising:

(a) storing programmable information; and

(b) generating a plurality of output clocks [using] with a phase lock loop (PLL), each of said output clocks being:

(i) capable of oscillating at a different one of a plurality of frequencies, and

(ii) generated in response to a reference clock frequency and one or more programming inputs.

13 ~~16~~. (Amended) A method according to claim ~~15~~ 12, further [16] comprising:

[generating a] (c) individually programming each of said plurality of output clocks [that are individually programmable] to one of a plurality of independent frequencies.

14 ~~17.~~ (Amended) A method according to claim ~~16~~ 13 further comprising:

(d) adjusting the impedance of said output clocks in response to said one or more programming inputs to match the impedance of an external device.

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15 ~~18.~~ (Amended) A method according to claim ~~16~~ 13 further comprising:

af cont.

[generating] (e) selecting said reference clock frequency [in response to] from one or more [internally generated] clocks generated internally to said programmable device.

16 ~~19.~~ (Amended) A method according to claim ~~16~~ 13 further comprising:

[generating] (e) selecting said reference clock frequency [in response to] from one or more [externally generated] clocks generated externally to said programmable device.

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17 ~~20.~~ (Amended) A method according to claim ~~16~~ 13 further comprising:

[generating] selecting said reference clock frequency [in response to] from one or more clocks generated internally [and] or externally [generated clocks] to said programmable device.

REMARKS

Careful review and examination of the subject application are noted and appreciated. For example, please note the change of power of attorney (and corresponding new address) acknowledged by the Patent Office in Paper No. 3, mailed April 14, 1997. Also, future correspondence should reflect a new attorney docket number, 0325.00063. Applicant's representative appreciates the United States Patent and Trademark Office's cooperation and understanding regarding this issue.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 5-6, 8-9, 11 and 14-20 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

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